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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,658	06/11/2001	Takahide Ohkami	264/087	2956

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,658	OHKAMI, TAKAHIDE	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,7 and 10* is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2001 and 22 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-7 and 10 of U.S. Application 09/879,658, originally filed on 06/11/2001 are currently pending. The application claims priority to provisional application 60/242,407, filed on 10/20/2000. Claim 10 was previously allowed.
2. Examiner finds that Applicant's arguments presented in the Appeal Brief filed on 10/31/05 are persuasive, in particular the arguments on pp.13-15 regarding claim 1, and the arguments on pp.21-22 regarding claim 6.
3. The finality of the previous Office Action is withdrawn. New art rejections have been applied.

Allowable Subject Matter

4. Claims 6-7 are allowed. The Beardslee reference expressly teaches (see col.13, lines 53-67) the following regarding design instrumentation circuitry (DIC) that is synthesized into the target logic design:

> Design instrumentation (DI) is a process by which a HDL description of an electronic system is analyzed, and then a DIC computed. The DIC is thereafter incorporated (e.g., added) into the electronic system to facilitate debugging. The DIC can be added to the electronic system in a variety of ways. In one embodiment, DIC can be added to the electronic system by adding an HDL description of the DIC to the HDL description of the electronic system. In another embodiment, the DIC can be added to the electronic system during synthesis. The DIC provides mechanisms to control the examination and/or modification of a running electronic system. Thus, the DIC allows to analyze, diagnose, and/or debug the DUT by giving detailed and accurate information about its current state of operation, as well as the state history.

However, Beardslee does not expressly teach that the DIC contains the "protocol logic synthesized into the target logic circuit design", as claimed in Claim 6 in the instant application. Claim 6 is therefore allowable. Dependent claim 7 depends from allowable Claim 6.

5. Claim 10 is allowed. In the previous Office Action, Claim 10 was objected to as being dependent upon a rejected base claim. The previously cited prior art (Sample, Koch, Patel, X.25), and the newly cited prior art (Beardslee) do not expressly teach, either individually or in combination, the following limitations:

> creating a finite state machine to indicate that the packet-based protocol logic is in either non-memory mode, continuous memory write mode, or continuous memory read mode; and
>
> creating a state transition control that selects said non-memory mode when said continuous memory operation ends, said state transition control further selecting said continuous memory write mode when said continuous memory write operation is initiated, said state transition control further selecting said continuous memory read mode when said continuous memory read operation is initiated.

Applicants have amended Claim 10 to incorporate the limitations of base Claim 9.

Preamble of the Claims

6. The preamble of Claim 1, as presented for examination, has not been given patentable weight. Appropriate weight is given to limitations recited in the body of the claim that are needed for purpose of antecedence. "A mere statement of purpose or intended use in the preamble of a claim need not be considered in finding anticipation; however, it must be considered if the language of a preamble is necessary to give meaning to the claim" *Diversitech Corp. v. Century Steps,*

Inc., 7 USPQ2d 1315 (Fed. Cir. 1988); In re Stencel, 4 USPQ2d 1071 (Fed. Cir. 1987).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. The prior art used for these rejections is as follows:

9. Beardslee et al., U.S. Patent 6,618,839. (Henceforth referred to as "**Beardslee**").

10. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

11. **Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Beardslee.**

12. In regards to Claim 1, Beardslee teaches the following limitations:

> 1. (Currently Amended) A method for compiling a user's logic design for implementation into a functional verification system such that communication bandwidth is increased between the functional verification system and a host workstation by allowing for greater read and write access to memories and registers in the user's logic design, comprising;
>
> identifying all of the memories and registers in the user's logic design;
>
> synthesizing accessibility logic into the user's logic design such that the user's logic design supplemented by said accessibility logic,
>
> said accessibility logic creating access ports to the memories and registers in the user's logic design,

the access ports facilitating writing of data received from the host workstation to the memories and registers in the user's logic design,

said access ports further facilitating reading of data stored in the memories and registers in the user's logic design for transfer to the host workstation.

The Beardslee reference expressly teaches (see col.13, lines 21-67; and Fig.2) design instrumentation circuitry (DIC) that is synthesized into the target logic design. In particular, Beardslee teaches (see col.13, lines 53-67):

> Design instrumentation (DI) is a process by which a HDL description of an electronic system is analyzed, and then a DIC computed. The DIC is thereafter incorporated (e.g., added) into the electronic system to facilitate debugging. The DIC can be added to the electronic system in a variety of ways. In one embodiment, DIC can be added to the electronic system by adding an HDL description of the DIC to the HDL description of the electronic system. In another embodiment, the DIC can be added to the electronic system during synthesis. The DIC provides mechanisms to control the examination and/or modification of a running electronic system. Thus, the DIC allows to analyze, diagnose, and/or debug the DUT by giving detailed and accurate information about its current state of operation, as well as the state history.

In particular, the cited section of Bearslee teaches:

> Thus, the DIC allows to analyze, diagnose, and/or debug the DUT by giving detailed and accurate information about its current state of operation, as well as the state history.

Examiner finds that facilitating the reading and writing of data into the memories and registers in the user's logic design are inherent in this teaching, because otherwise it would impossible to give "detailed and accurate information about [the DUT's] current state of operation, as well as the state history"

13. In regards to Claim 2, Beardslee teaches (See col.16, lines 44-52) the following limitations:

> 2. (Currently Amended) The method of claim 1 further comprising the step of assigning a unique identifier to each of the memories and registers in the user's logic design.

In particular, the cited section of Bearslee teaches:

> Following operation 424, as well as following the decision 422 when instrumented, pre-designed blocks are not provided, DIC information is stored 426 to a design instrumentation database. The DIC information includes a description of the DIC, the instrumentation directives, and DIC connectivity information. The DIC information can also include cross-reference data that relates elements in the design of the electronic system (i.e., hardware implementation) to and from the HDL description.

14. In regards to Claim 3, Beardslee teaches (See col.17, lines 18-22) the following limitations:

> 3. (Currently Amended) The method of claim 2 wherein said accessibility logic comprises selecting logic,
>
> said selecting logic adapted to receive said unique identifier and select a particular one of the memories and registers in the user's logic design.

In particular, the cited section of Bearslee teaches:

> In one embodiment, DV is done by sampling the values of one or more signals of the DUT for a particular time interval determined by one or more predetermined events.

Examiner interprets that the selecting logic is inherent in inherent in Bearslee's DV sampling of "one or more signals ... determined by one or more predetermined events."

15. In regards to Claim 4, Beardslee teaches the following limitations:

> 4. (Currently Amended) The method of claim 3 wherein said accessibility logic comprises logic to read from or write to said particular one of the memories and registers in the user's logic design.

In particular, the cited section of Bearslee teaches:

> In one embodiment, DV is done by sampling the values of one or more signals of the DUT for a particular time interval determined by one or more predetermined events.

Examiner interprets that the selecting logic is inherent in inherent in Bearslee's DV sampling of "one or more signals ... determined by one or more predetermined events."

16. In regards to Claim 5, Beardslee teaches the following limitations:

> 5. (Currently Amended) The method of claim 4 wherein said accessibility logic comprises decode logic that receives commands from a host and controls execution of reading and writing data to the memories and registers in the user's logic design.

In particular, the cited section of Bearslee teaches:

> In one embodiment, DV is done by sampling the values of one or more signals of the DUT for a particular time interval determined by one or more predetermined events.

Examiner interprets that the decoding logic is inherent in inherent in Bearslee's DV sampling of "one or more signals ... determined by one or more predetermined events."

Conclusion

17. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

18. U.S. Patent 6,931,572 to Schubert et al. (A patent by the same inventors as the Beardslee patent, with the same filing date, and very similar teachings).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (571) 273-8300, or mailed to:

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Alexandria, VA 22313-1450

or hand carried to:

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Customer Service Window
Randolph Building
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Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon
Art Unit 2123
January 13, 2006

Paul L. Rodriguez 1/18/06
Primary Examiner
Art Unit 2125